

Seminar

Fall 2011



THE UNIVERSITY OF
SOUTHERN MISSISSIPPI
SCHOOL OF COMPUTING

Title: High Performance Computing using
the Intel Advanced Vector Extensions

Time & Location:

2:00pm, Friday, September 23, 2011
Tec 205 (Vislab), Bobby Chain Technology Building

Presenter:

Dr. Benjamin Seyfarth
School of Computing
The University of Southern Mississippi

Abstract: The latest Intel CPUs (Core i3, i5 and i7) include vector instructions operate on 256 bit registers. These registers can be used as eight 32 bit floating point values or four 64 bit floating point values. This means that one instruction can perform either 8 or 4 floating point operations. In addition the instructions are pipelined which permits the CPU to complete one instruction per cycle. Lastly if the instructions are somewhat independent the CPU can perform instructions in multiple pipelines simultaneously, making it possible to complete more than four double precision floating point operations per cycle.

The talk will start with some simple examples illustrating the AVX instructions and basic concepts for high performance. The final example will be a high performance implementation computing correlation between 2 double precision arrays.